An Enhanced 130 nm Generation Logic Technology Featuring 60 nm Transistors Optimized for High Performance and Low Power at 0.7 - 1.4 V

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Abstract

A leading edge 130 nm technology with 6 layers of Cu interconnects and 1.3 V operation has previously been presented [1]. In this work we enhance the previous technology with the following: transistor improvements which support a 60 nm gate dimension and increased drive current, improved 6-T SRAM device matching to allow low power and high performance operation from 0.7 to 1.4 V, 5% linear shrink to reduce the 6-T SRAM cell to 2.00 um ^{2} while still using 248 nm lithography. Saturation drive currents of 1.30 mA/um for N-channel and 0.66 mA/um for P-channel low V_T devices are the highest reported to date and represent a 11 % improvement over what was published in [1]. Excellent device short channel effects are obtained for the 60 nm gate length devices as measured by the 270 mV threshold voltage and <100 mV/V DIBL. These results have been achieved on both 200 and 300 mm wafers.

Introduction

Typical microprocessor power levels have increased from a few to > 40 Watts over the past 15 years due to increasing transistor count and clock frequencies. The increasing power has occurred even though the energy per gate switching transition has decreased approximately $(0.7)^3$ per technology node due to voltage scaling and device area scaling. Figure 1 shows these trends for Intel's CMOS logic technology generations. In this paper we describe a 130 nm generation technology operating at 0.7 to 1.4 V for high speed and low power operation. To offer high performance over the entire voltage range, this technology offers low transistor threshold voltages of 300 mV (high V_{TN}) and 270 mV (low V_{TN}) while maintaining I_{OFF} of 10 nA/um and 100 nA/um, excellent DIBL at <100 mV/V) which allows for not only high saturation drive currents but equally important high linear drive currents, high surface channel mobility for 1.5 nm gate oxides, all at aggressive 60 nm nominal gate lengths.

Process Flow and Technology Features

Front-end technology features include shallow trench isolation, retrograde wells, shallow abrupt source/drain extensions, halo implants, deep source/drain, and cobalt salicidation. The minimum pitches and thicknesses for the technology layers are summarized in Table 1. They result from a 5% linear shrink and more aggressive contact and metal 1 pitch to enable a 2.00 um ^{2} 6-T SRAM cell (1.22 x 1.64 um). Figure 2 shows a top down SEM of the polysilicon gate conductor and the metal 1 connections. The interconnect technology uses dual damascene copper to reduce the resistances of the 6 layers of interconnects. Fluorinated SiO_2 is used as inter-level dielectric (k is measured to be 3.6).

LAYER	PITCH	THICK	AR
Isolation	**345**	**450**	**-**
Polysilicon	**319**	**160**	**-**
Metal 1	**293**	**280**	**1.7**
Metal 2,3	**425**	**360**	**1.7**
Metal 4	**718**	**570**	**1.6**
Metal 5	**1064**	**900**	**1.7**
Metal 6	**1143**	**1200**	**2.1**

Table 1: Layer pitch, thickness (nm) and aspect ratio.

Transistor Features

(a) Gate Length Dimension: Figure 3 shows a cross-sectional TEM for a transistor with a 60 nm gate length and straight poly-Si side wall profile as opposed to the notched poly used in the 180 nm node [2]. Straight sidewall gates were chosen at the 130 nm node since the source drain extension does not have to diffuse under the notch, thus allowing for shallower junctions to be fabricated. At aggressive gate lengths of 60 nm, controlling short channel effects at low threshold voltage by shallow junctions and abrupt halo doping is key to achieving high linear and saturation drive current.

(b) 1.5nm Physical Gate-Oxide: In order to achieve high drive current and minimize short channel effects a gate oxide process with 1.5 nm physical thickness was developed which meets performance, reliability, and manufacturability criteria (Figure 4). High electron and hole mobilities are required to achieve high linear drive current, which can be missed in technology optimization since transistor linear current is not reflected in a simple CV/I metric. Concerns have been raised that in ultra-thin oxides, gate electrode to oxide interface scattering and high fixed charge due to nitridation reduces mobility. The measured mobility dependence on the effective oxide field, shown in Figure 5, demonstrates that high electron and hole mobilities can be achieved for well-

optimized gate oxides with 1.5 nm thickness.

(C) Well-Halo and SD-Extension Engineering: A simple but ineffective way to offer high saturation drive current at small gate lengths is to use high well doping to raise the threshold voltage to control short channel effects. This approach offers low CV/I but does not improve product performance for two reasons. First, the linear drive current will be significantly degraded (saturated drive current is not degraded at a fixed I_{OFF} due to high DIBL). Second, the high well doping leads to increased threshold voltage variations due to gate length variation (present in the range of +/- 10% L_{GATE} for a modern technology). In this work we use retrograde wells, low energy high angle abrupt halo implants with shallow junctions formed by low diffusion processing to control short channel effects. Figure 6 shows the N-channel threshold voltage versus gate length resulting in a linear threshold voltages of 300 and 270 mV at 60 nm gate length for the high and low threshold devices, respectively. From Figure 6, DIBL for the 60 nm NMOS devices are measured to be <100 mV/V for high and low threshold devices. Similar results have been achieved for p-channel devices.

High V_T saturation drive currents are 1.14 mA/um for N-channel and 0.56 mA/um for P-channel devices (Figure 7). Low V_T drive currents are 1.30 mA/um for N-channel and 0.66 mA/um for P-channel devices (Figure 8). Subthreshold slopes for both N-channel and P-channel high and low threshold devices remain well controlled at less than 85 mV/decade at L_{GATE}=60 nm (Figure 9). The I_{ON}/I_{OFF} ratio remains high for the aggressively scaled power supply voltage of 1.4 V (Figure 10). Table 2 shows the transistor I_{ON} and I_{OFF} at 0.7 and 1.4 V.

DEVICE	VDD (V)	I_{OFF} (N) (nA/um)	I_{ON} (N) (mA/um)	I_{ON}(P) (mA/um)
Low V_T	**1.4**	**100**	**1.30**	**0.66**
High V_T	**1.4**	**10**	**1.14**	**0.56**
Low V_T	**0.7**	**20**	**0.37**	**0.19**
High V_T	**0.7**	**2**	**0.32**	**0.16**

Table 2: I_{ON} and I_{OFF} at 0.7 and 1.4V V_{DD}

In a modern microprocessor with 6 layers of interconnects, transistor loads are comprised of > 50% interconnect capacitance. To obtain high product performance it is necessary to provide transistors with more than low CV/I but also high saturation and linear drive current. Figure 11 shows the recent trend of saturation drive currents for Intel's process technologies. This work extends the trend to offer the highest drive current to date of 1.30 mA/um for low threshold N-channel device.

Performance Metrics

Figure 12 shows measured inverter gate delay vs n-channel off state leakage for unloaded ring oscillator (fan out =1) operating at 1.4 V at room temperature. PMOS off state leakage is fixed at 10 nA/um for these devices. The delay per stage at 1.4 V falls below 6 psec when the off state leakage is about 10 nA/um.

Power consumption is a growing concern for high performance microprocessors with increasing clock frequency and transistor count. The best way to reduce power is to operate at a low supply voltage. Figure 13 shows that by improving device matching and eliminating defects which cause device mismatch, a 18Mb SRAM fabricated in this technology can operate at voltage down to 0.5 V. A metric, which comprehends both power and speed, is the energy-delay product. Figure 14 shows the estimated NMOS energy delay product for a large number of published devices [3] and for the devices reported in this work. As evident from Figure 14, The NMOS energy-delay product is better than the published industry trend.

A 18 Mbit CMOS SRAM, Pentium® 3 (Figure 15) and 4 microprocessor were fabricated and used as a yield and reliability test vehicles during the process development. The SRAM and microprocessor die yields are equivalent or better than past technologies at this point of time relative to ramping in high volume manufacturing. The Pentium® 4 performance is measured using the maximum clock frequency of operation. Figure 16 shows the schmoo plot for the Pentium® 4, i.e the maximum frequency as a function of voltage. At 1.4 V operation, the present design version of the Pentium® 4 has a clock frequency of 2.5 Ghz.

Conclusion

A 130nm generation logic technology has been developed and is in high volume manufacturing with high performance transistors that can operate in the range of 0.7 and 1.4 V. The technology performance capabilities are demonstrated with ring oscillator delays of 6 ps/stage and with a Pentium® 4 operating at 2.5 GHz.

Acknowledgement

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References

[1] S. Tyagi et. al, IEDM Tech. Digest, pp 567-571 (2000).

[2] T. Ghani et. al, IEDM Tech. Digest, pp 415-419 (1999).

[3] M. Bohr, IEDM Tech. Digest, pp 273-277, (1994).

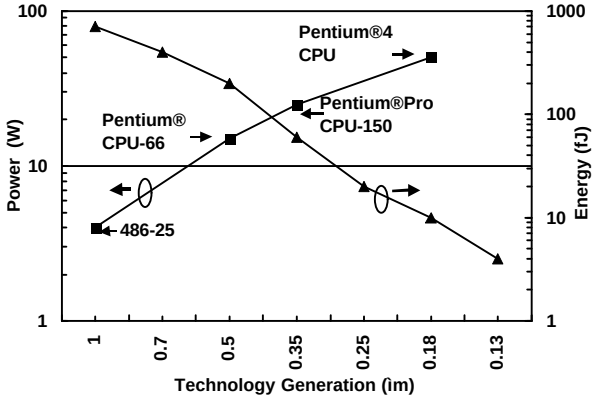

Figure 1: Transistor switching energy and CPU power trends

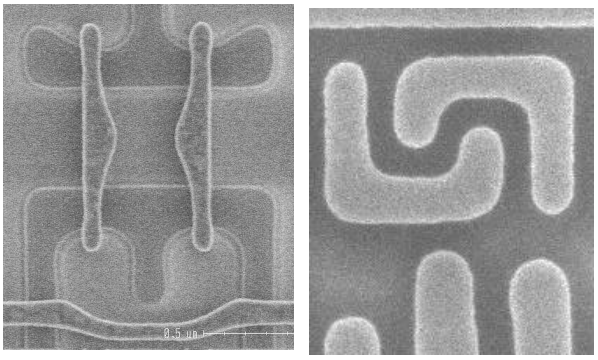

Figure 2: 2.00um^2 6-T SRAM cell at poly gate layer (left) and metal 1 (right)

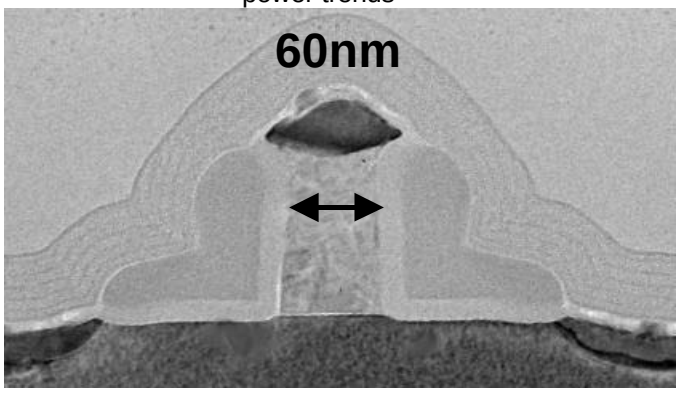

Figure 3: TEM cross-section of 60nm NMOS

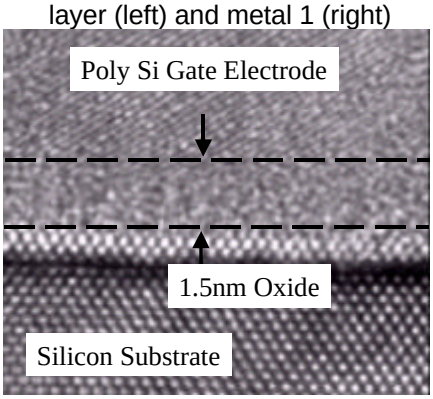

Figure 4: TEM of 1.5nm physical gate oxide

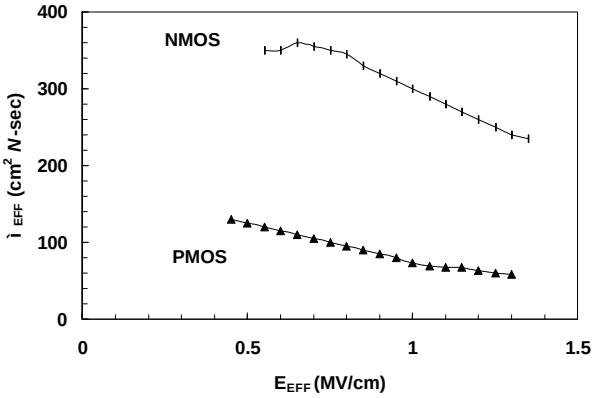

Figure 5: Mobility vs. effective electric field

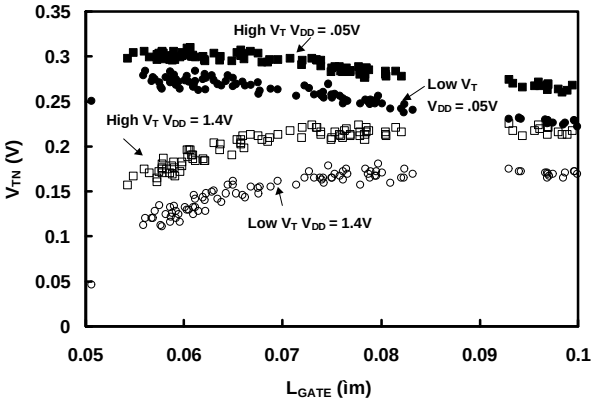

Figure 6: V_{TN} vs L_{GATE}

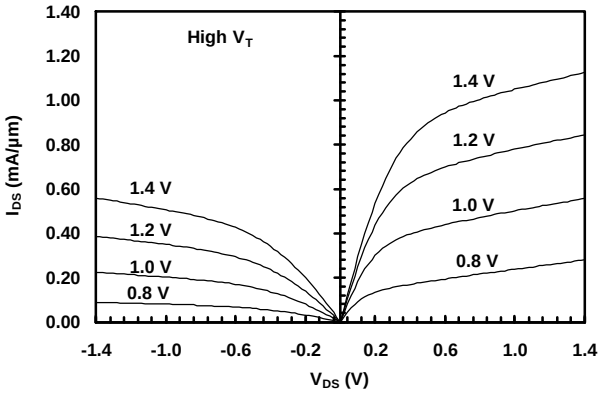

Figure 7: I-V curves for high V_T device (L_{GATE}=60 nm)

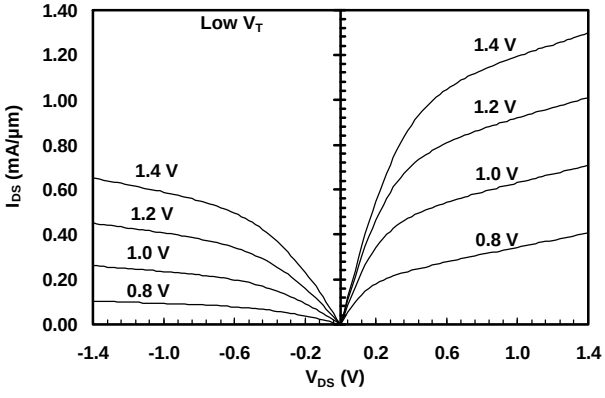

Figure 8: I-V curves for low V_T device (L_{GATE}=60 nm)

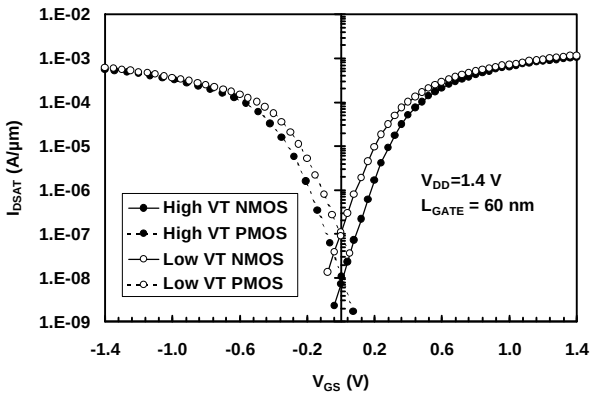

Figure 9: Sub-threshold characteristics

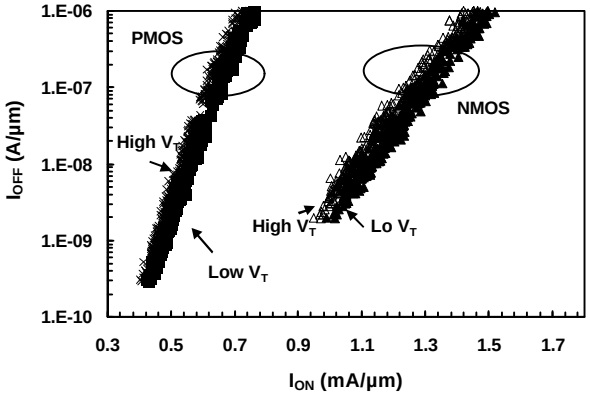

Figure 10: I_{ON} versus I_{OFF} (V_{DD} =1.4V)

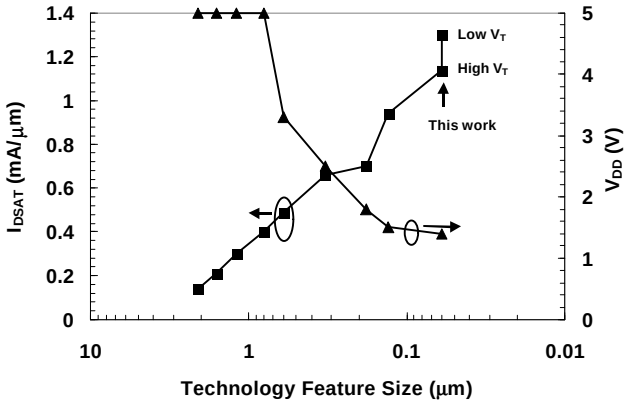

Figure 11: Intel NMOS I_{DSAT} trend

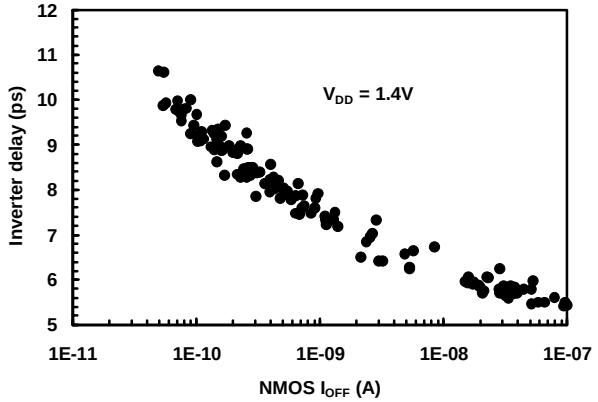

Figure 12: Inverter delay (PMOS I_{OFF} =10 nA/um)

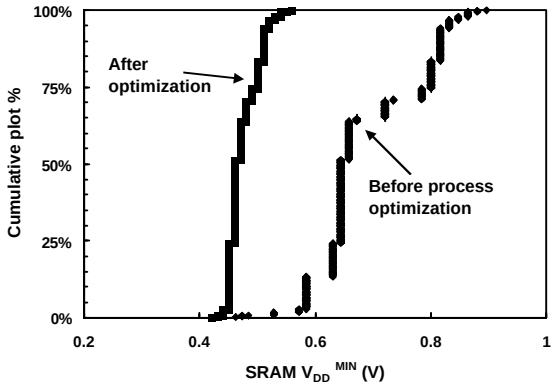

Figure 13: SRAM operation vs voltage

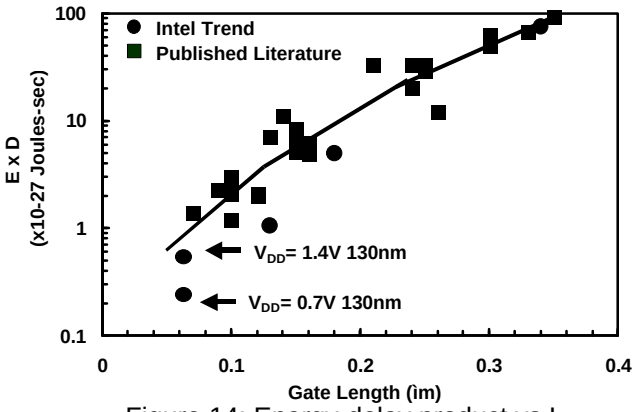

Figure 14: Energy-delay product vs L_{GATE}

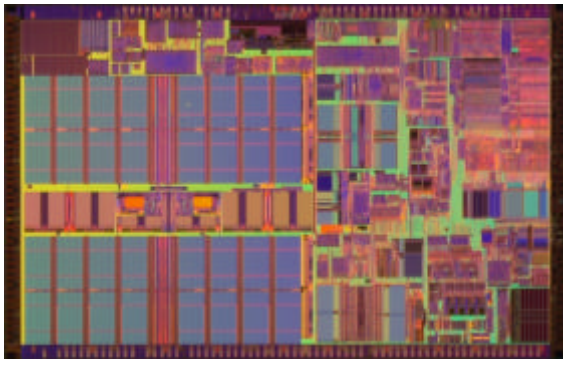

Figure 15: Pentium® III die photo

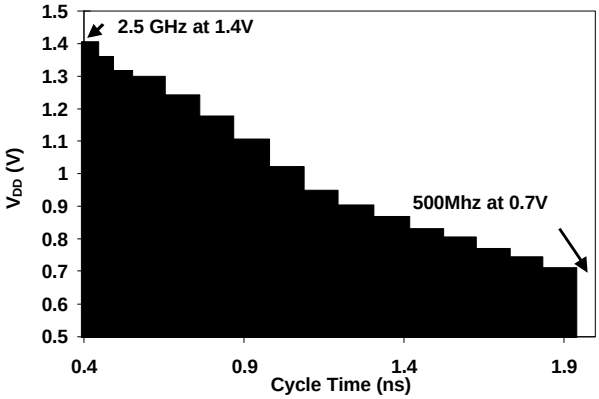

Figure 16: Fmax schmoo plot for Pentium® 4